JYJE1533

20 ppm, Ultra-Low Power 32.768 kHz Quartz XTAL Replacement

Features

- Small SMD package: 2.0 x 1.2 mm (2012)[1]
- Pin-compatible to 2012 XTAL SMD package
- Fixed 32.768 kHz output frequency
- <20 ppm frequency tolerance Ultra-low power: <1 µA
- Supports coin-cell or super-cap battery backup voltages
- Vdd supply range: 1.5V to 3.63V over -40°C to +85°C
- Oscillator output eliminates external load caps
- Internal filtering eliminates external Vdd bypass cap
- NanoDrive™ programmable output swing for lowest power
- Pb-free, RoHS and REACH compliant

Applications

- Mobile Phones
- Tablets
- Health and Wellness Monitors
- Fitness Watches
- Sport Video Cams
- Wireless Keypads
- Ultra-Small Notebook PC
- Pulse-per-Second (pps) Timekeeping
- RTC Reference Clock
- Battery Management Timekeeping

Note:

1. For the smallest 32 kHz XO in CSP (1.2 mm^2), consider the JYJE1532.

Electrical Specifications

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Fixed Output Frequency	Fout		32.768		kHz	
Frequency Stability						
Frequency Tolerance[2]	F_tol			20	ppm	T_A = 25°C, post reflow, Vdd: 1.5V – 3.63V.
Frequency Stability[3]	F_stab			75	ppm	T_A = -10°C to +70°C, Vdd: 1.5V – 3.63V.
				100		T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V.
				250		T_A = -10°C to +70°C, Vdd: 1.2V – 1.5V.
25°C Aging		-1		1	ppm	1st Year
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.2		3.63	V	T_A = -10°C to +70°C
		1.5		3.63	V	T_A = -40°C to +85°C
Core Operating Current[4]	Idd		0.90		µA	T_A = 25°C, Vdd: 1.8V. No load
				1.3		T_A = -10°C to +70°C, Vdd max: 3.63V. No load
				1.4		T_A = -40°C to +85°C, Vdd max: 3.63V. No load
Output Stage Operating Current[4]	Idd_out		0.065	0.125	µA/Vpp	T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V. No load
Power-Supply Ramp	t_Vdd_ Ramp			100	ms	T_A = -40°C to +85°C, 0 to 90% Vdd
Start-up Time at Power-up[5]	t_start		180	300	ms	T_A = -40°C ≤ T_A ≤ +50°C, valid output
				450		T_A = +50°C < T_A ≤ +85°C, valid output
Operating Temperature Range						
Commercial Temperature	T_use	-10		70	°C	
Industrial Temperature		-40		85	°C	

Notes:

2. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
3. Stability is specified for two operating voltage ranges. Stability progressively degrades with supply voltage below 1.5V. Measured peak -to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load.
4. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + (0.065 µA/V) * (peak-to-peak output Voltage swing).
5. Measured from the time Vdd reaches 1.5V.

Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Option, T_A = -40°C to +85°C, typical values are at T_A = 25°C						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF load, Vdd = 1.5V to 3.63V
				50		10-90% (Vdd), 5 pF load, Vdd ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -10 µA, 15 pF
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 10 µA, 15 pF
NanoDrive™ Programmable, Reduced Swing Output						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	JYJE1533 does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 2 for acceptable NanoDrive swing options. Vdd: 1.5V – 3.63V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA.
DC-Biased Programmable Output Voltage High Range	VOH		0.60 to 1.225		V	Vdd: 1.5V – 3.63V. I_{OH} = -0.2 µA, 10 pF Load. See Table 1 for acceptable V_{OH}/V_{OL} setting levels.
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	Vdd: 1.5V – 3.63V. I_{OL} = 0.2 µA, 10 pF Load. See Table 1 for acceptable V_{OH}/V_{OL} setting levels.
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, Vdd = 1.5V to 3.63V.
Period Jitter	T_jitt		35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V

Table 2. Pin Configuration

SMD Pin	Symbol	I/O	Functionality
1	NC	No Connect	No Connect. Will not respond to any input signal. When interfacing to an MCU's XTAL input pins, this pin is typically connected to the receiving IC's X Out pin. In this case, the JYJE1533 will not be affected by the signal on this pin. If not interfacing to an XTAL oscillator, leave pin 1 floating (no connect).
2	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground.
3	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The JYJE1533 oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
4	Vdd	Power Supply	Connect to power supply 1.5V ≤ Vdd ≤ 3.63V for operation over -40°C to +85°C temperature range. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). Internal power supply filtering will reject more than ±150 mVpp with frequency components through 10 MHz. Contact JYJE for applications that require a wider operating supply voltage range.

SMD Package (Top View)

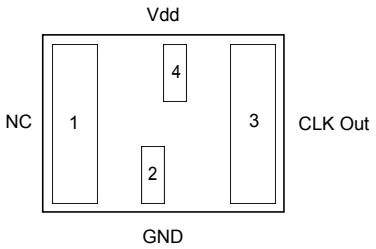


Figure 1. Pin Assignments

System Block Diagram

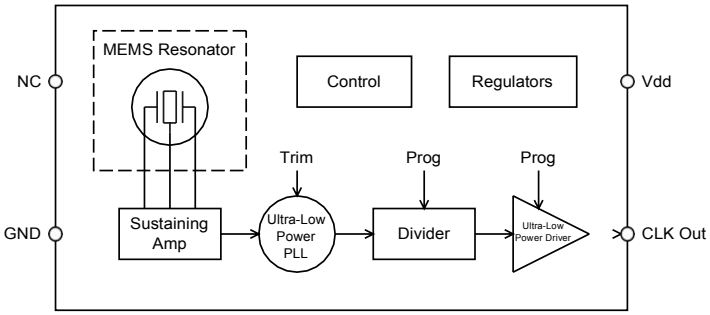


Figure 2. JYJE1533 Block Diagram

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes, over -40°C to +85°C	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model ESD Protection	HBM, JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD220C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
2012 SMD Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

Description

The JYJE1533 is an ultra-small and ultra-low power 32.768 kHz oscillator optimized for mobile and other battery-powered applications. The JYJE1533 is pin-compatible and footprint compatible to existing 2012 XTALs when using the JYJE solder-pad layout (SPL). And unlike standard oscillators, the JYJE1533 features NanoDrive™, a factory programmable output that reduces the voltage swing to minimizepower.

The 1.2V to 3.63V operating supply voltage range makes it an ideal solution for mobile applications that incorporate a low-voltage, battery-back-up source such as a coin-cell or super-cap.

JYJE's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with JYJE's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, JYJE's MEMS resonator die can be used like any other semiconductor die. One unique result of JYJE's MEMS First and EpiSeal manufacturing processes is the capability to integrate JYJE's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

XTAL Footprint Compatibility (SMD Package)

The JYJE1533 is a replacement to the 32 kHz XTAL in the 2.0 x 1.2 mm (2012) package. Unlike XTAL resonators, JYJE's silicon MEMS oscillators require a power supply (Vdd) and ground (GND) pin. Vdd and GND pins are conveniently placed between the two large XTAL pins. When using the JYJE Solder Pad Layout (SPL), the JYJE1533 footprint is compatible with existing 32 kHz XTALs in the 2012 SMD package. Figure 3 shows the comparison between the quartz XTAL footprint and the JYJE footprint. For applications that require the smallest footprint solution, consider the JYJE1532 XO available in a 1.2mm^2 CSP.

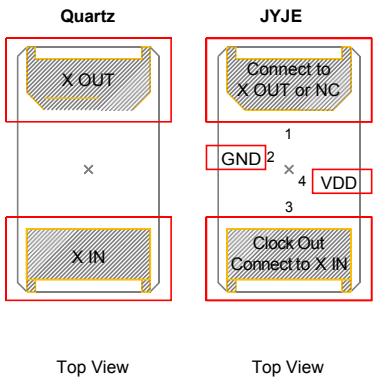


Figure 3. JYJE1533 Footprint Compatibility with Quartz XTAL Footprint[6]

Frequency Stability

The JYJE1533 is factory calibrated (trimmed) to guarantee frequency stability to be less than 20 ppm at room temperature and less than 100 ppm over the full -40°C to +85°C temperature range. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point, the JYJE1533 temperature coefficient is extremely flat across temperature. The device maintains less than 100 ppm frequency stability over the full operating temperature range when the operating voltage is between 1.5 and 3.63V as shown in Figure 4.

Functionality is guaranteed over the 1.2V – 3.63V operating supply voltage range. However, frequency stability degrades below 1.5V and steadily degrades as it approaches the 1.2V minimum supply due to the internal regulator limitations. Between 1.2V and 1.5V, the frequency stability is 250 ppm max over temperature.

When measuring the JYJE1533 output frequency with a frequency counter, it is important to make sure the counter's gate time is >100ms. The slow frequency of a 32 kHz clock will give false readings with faster gate times.

Contact JYJE for alternative 32 kHz product options and applications that require a wider supply voltage range >3.63V, or operating frequency below 32 kHz.

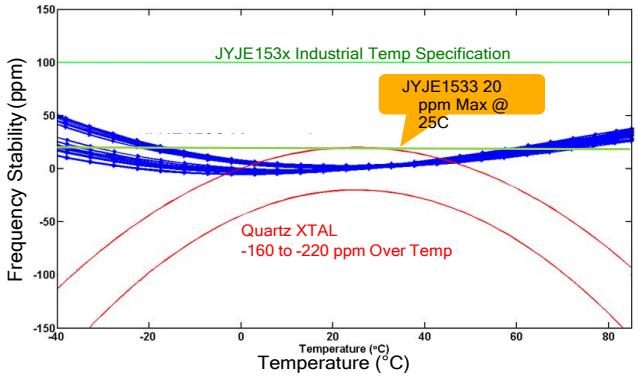


Figure 4. JYJE vs. Quartz

Power Supply Noise Immunity

The JYJE1533 is an ultra-small 32 kHz oscillator. In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor. This feature further simplifies the design and keeps the footprint as small as possible. Internal power supply filtering is designed to reject AC-noise greater than ±150 mVpp magnitude and beyond 10 MHz frequency component.

Output Voltage

The JYJE1533 has two output voltage options.

One option ia standard LVCMOS output swing. The second option is the NanoDrive reduced swing output.Output swing is customer specific and programmedbetween 200 mV and 800 mV. For DC-coupled applications,

output VOH and VOL are individually factory programmed to the customers'

requirement. VOH programming range is between 600 mV and 1.225V in 100 mV increments. Similarly, VOL programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2V VIH and a 0.6V VIL.

Simply select JYJE1533 NanoDrive factory programming code to be “D14” and the correct output thresholds will match the downstream PMIC or MCU input requirements. Interface logic will vary by manufacturer and we recommend that you review the input voltage requirements for the input interface.

For DC-biased NanoDrive output configuration, the minimum VOL is limited to 350mV and the maximum allowable swing (VOH - VOL) is 750mV. For example, 1.1V VOH and 400mV VOL is acceptable, but 1.2V VOH and 400 mV VOL is not acceptable.

When the output is interfacing to an XTAL input that is internally AC-coupled, the JYJE1533 output can be factory programmed to match the input swing requirements. For example, if a PMIC or MCU input is internally AC-coupled and requires an 800mV swing, then simply choose the JYJE1533 NanoDrive programming code “AA8” in the part number. It is important to note that the JYJE1533 does not include internal AC-coupling capacitors. Please see the Part Number Ordering section at the end of the datasheet for more information about the part number ordering scheme.

Power-up

The JYJE1533 starts-up to a valid output frequency within 300 ms (150ms typ). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd). Start-up time is measured from the time Vdd reaches 1.5V. For applications that operate between 1.2V and 1.5V, the start-up time will be longer.

JYJE1533 NanoDrive™

Figure 5 shows a typical JYJE1533 output waveform (into a 10 pF load) when factory programmed for a 0.70V swing and DC bias (VOH/VOL) for 1.8V logic:

Example:

- NanoDrive™ part number coding: **D14**.
  Example part number: JYJE1533AI-H4-**D14**-32.768
- VOH = 1.1V, VOL = 0.4V (Vsw = 0.70V)

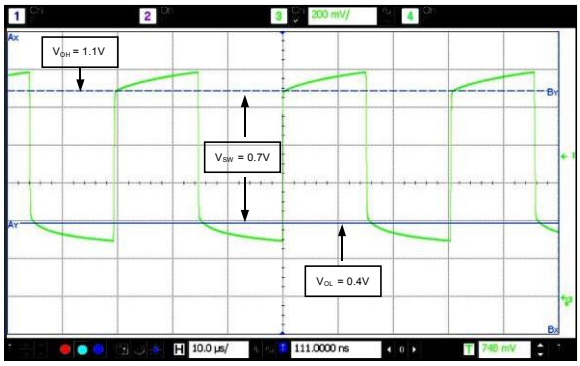


Figure 5. JYJE1533AI-H4-D14-32.768

Table 4 shows the supported NanoDrive™ VOH, VOL factory programming options.

Table 4. Acceptable VOH/VOL NanoDrive™ Levels

NanoDrive	V_{OH} (V)	V_{OL} (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8V logic compatible
D14	1.1	0.4	700 ±55	1.8V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

The values listed in Table 4 nominal values at 25°C and will exhibit a tolerance of ±55 mV across Vdd and -40°C to 85°C operating temperature range.

JYJE1533 Full Swing LVCMOS Output

The JYJE1533 can be factory programmed to generate full-swing LVCMOS levels. Figure 6 shows the typical LVCMOS waveform (Vdd = 1.8V) at room temperature into a 15 pF load.

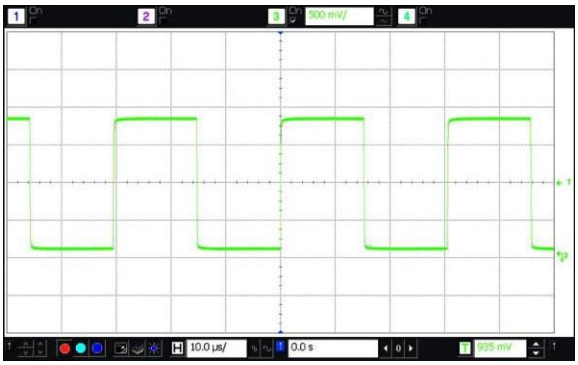


Figure 6. LVCMOS Waveform (Vdd = 1.8V) into 15 pF Load

Example:

- LVCMOS output part number coding is always **DCC**
- Example part number: JYJE1533AI-H4-**DCC**-32.768

Calculating Load Current

No Load Supply Current

When calculating no-load power for the JYJE1533, the core and output driver components need to be added. Since the output voltage swing can be programmed for reduced swing between 300 mV and 700 mV, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = Idd Core + (65nA/V)(Voutpp)

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 900nA (typ)
- Voutpp = 1.8V (LVCMOS)
- Supply Current = 900nA + (65nA/V)(1.8V) = 1017nA

Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8V
- Idd Core = 900nA (typ)
- Voutpp (D14) = V_{OH} – V_{OL} = 1.1V – 0.4V = 700mV
- Supply Current = 900nA + (65nA/V)(0.7V) = 946nA

Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below. Note the 27% reduction in power with a 1.8V logic compatible NanoDrive™ output voltage.

Total Current = Idd Core + Idd Output Driver (65nA/V*Voutpp) + + Load Current (C*V*F)

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 900nA
- Load Capacitance = 10pF
- Idd Output Driver: (65nA/V)(1.8V) = 117nA
- Load Current: (10pF)(1.8V)(32.768kHz) = 590nA
- Total Current = 900nA+117nA+590nA = 1.6µA

Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8V
- Idd Core = 900nA
- Load Capacitance = 10pF
- Voutpp (D14): V_{OH} – V_{OL} = 1.1V – 0.4V = 700mV
- Idd Output Driver: (65nA/V)(0.7V) = 46nA
- Load Current: (10pF)(0.7V)(32.768kHz) = 229nA

Total Current = 900nA + 46nA + 229nA = 1.175µA

Typical Operating Curves

(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)

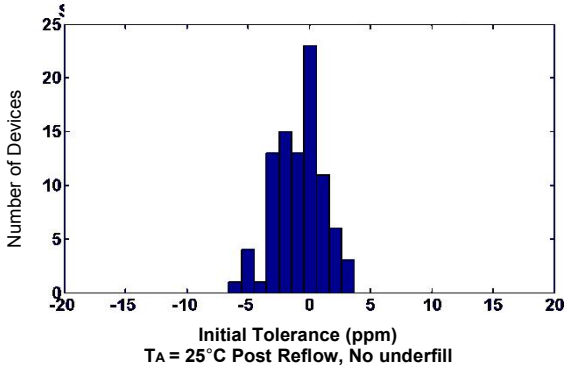


Figure 7. Frequency Stability Over Temperature (Pre-Reflow)

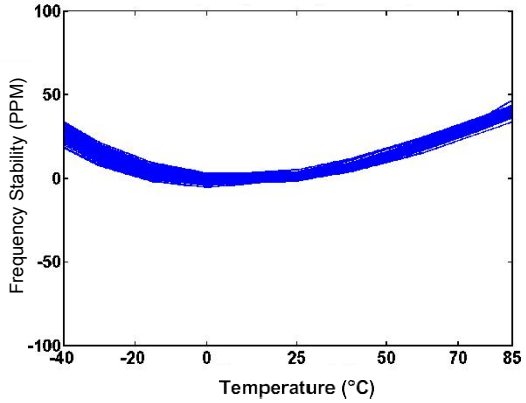


Figure 8. Frequency Stability over Temperature

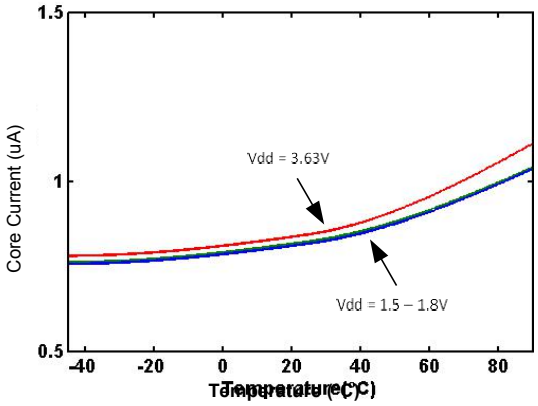


Figure 9. Core Current Over Temperature

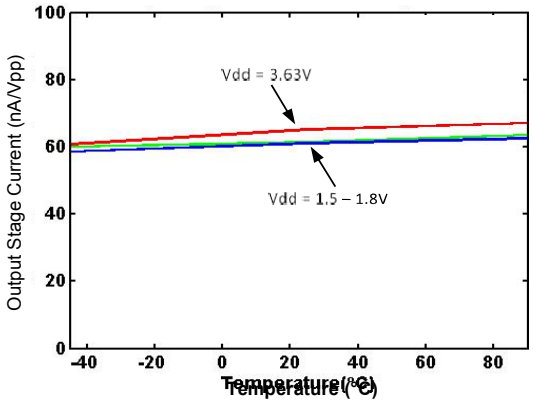


Figure 10. Output Stage Current Over Temperature

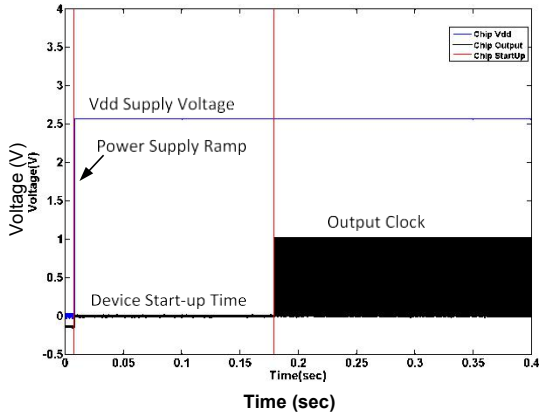


Figure 11. Start-up Time

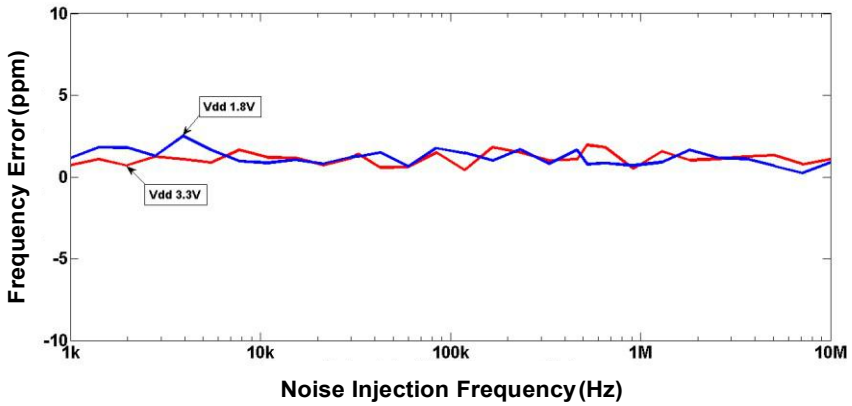


Figure 12. Power Supply Noise Rejection (±150mV Noise)

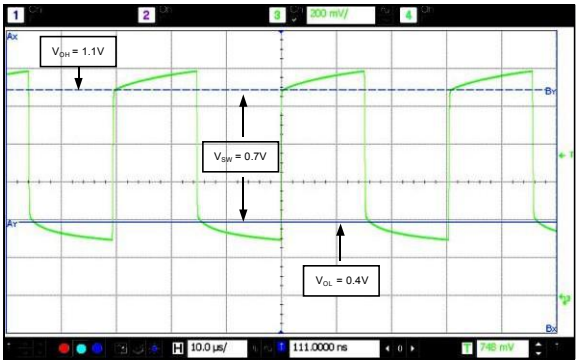


Figure 13. NanoDrive™ Output Waveform
(VOH = 1.1V, VOL = 0.4V; JYJE1533AI-H4-D14-32.768)

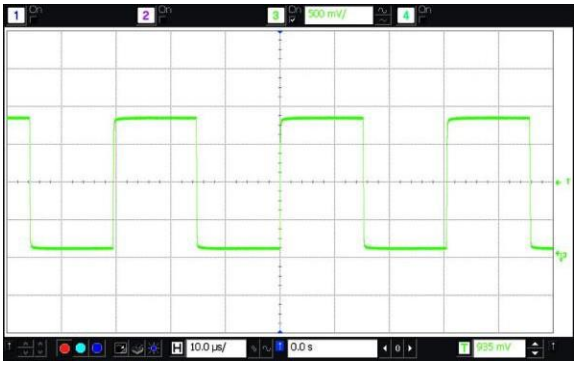
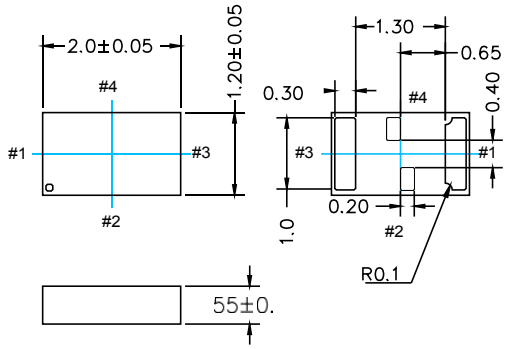
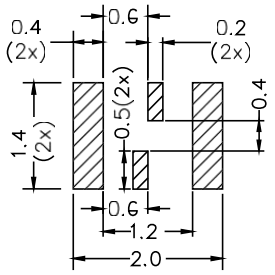
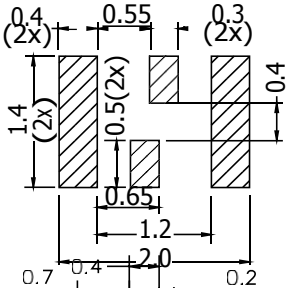
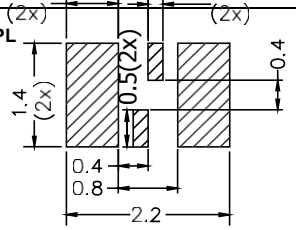


Figure 14. LVCMOS Output Waveform
(Vswing = 1.8V, JYJE1533AI-H4-DCC-32.768)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[7]	Recommended Land Pattern (Unit: mm)
2.0 x 1.2 mm SMD 	**JYJE Only SPL**  **JYJE Alternate SPL with Larger Center Pads**  **XTAL Compatible SPL** 

Note:

6. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.

Manufacturing Guidelines

1) No Ultrasonic Cleaning: Do not subject the JYJE1533 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.
2) For Noisy, high EM environments, we recommend the following design guidelines:
   - Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
   - Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the JYJE oscillator.
   - Add a low ESR/ESL, 0.1uF to 1.0uF ceramic capacitor (X7R) to help filter high frequency noise on the Vdd power-supply line. Place it as close to the JYJE oscillator Vdd pin as possible.
   - Place a solid GND plane underneath the JYJE oscillator to shield the oscillator from noisy traces on the other board layers.
   - For details, please refer to the PCB Layout Guidelines in AN10006.

For additional manufacturing guidelines and marking/tape-reel instructions.

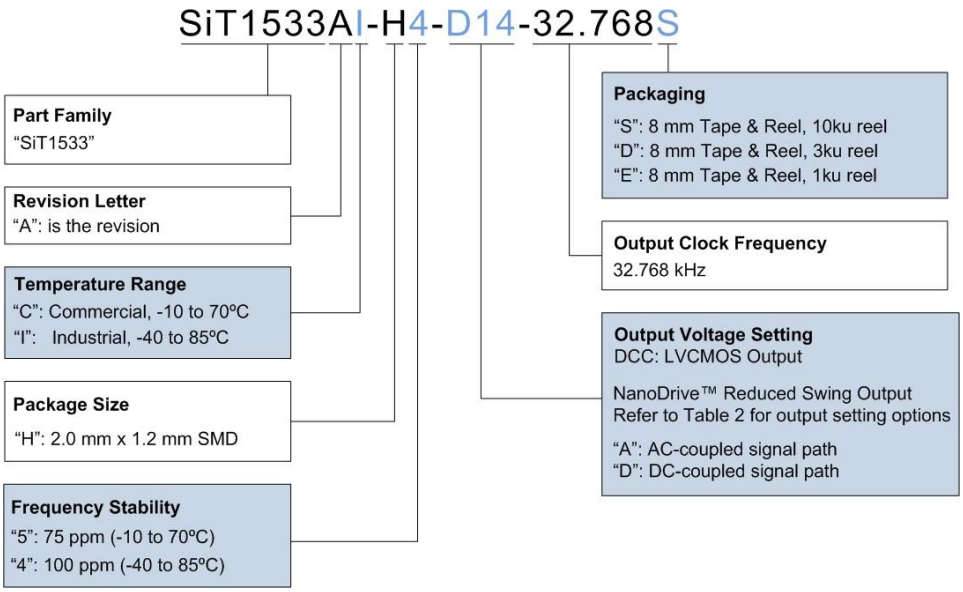
Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed. Here are guidelines to select the correct output voltage. These are only suggestions and specific chipsets may require different output voltage settings.

1) For XTAL replacement applications that will keep the chipset oscillator enabled, configure the NanoDrive™ output for a swing similar to the XTAL, approximately 300 mV.

   ⟶ JYJE1533AI-H4-AA3-32.768

2) For XTAL replacement applications that will disable the chipset oscillator, configure the output with one of the following:
   - For VDD = 1.8V: JYJE1533AI-H4-D14-32.768
   - For VDD > 1.8V: JYJE1533AI-H4-DCC-32.768



The following examples illustrate how to select the appropriate temp range and output voltage requirements:

Example 1: JYJE1533AI-H4-D14-32.768

- Industrial temp & corresponding 100 ppm frequency stability. Note, 100 ppm is only available for the industrial temp range, and 75 ppm is only available for the commercial temp range.
- Output swing requirements:
  a) "D" = DC-coupled receiver
  b) "1" = VOH = 1.1V
  c) "4" = VOL = 0.4V

Example 2: JYJE1533AC-H5-AA2-32.768

- Commercial temp & corresponding 75 ppm frequency stability. Note, 100 ppm is only available for the industrial temp range, and 75 ppm is only available for the commercial temp range.
- Output swing requirements:
  a) "A" = AC-coupled receiver
  b) "A" = AC-coupled receiver
  c) "3" = 300 mV swing

Table 5. Acceptable V_{OH}/V_{OL} NanoDrive™ Levels[8]

NanoDrive	V_{OH} (V)	V_{OL} (V)	Swing (mV)	Comments
D26	1.2	0.6	600 ±55	1.8V logic compatible
D14	1.1	0.4	700 ±55	1.8V logic compatible
D74	0.7	0.4	300 ±55	XTAL compatible
AA3	n/a	n/a	300 ±55	XTAL compatible

Note:

7. If these available options do not accommodate your application, contact Factory for other NanoDrive options.

Table 6. Revision History

Version	Release Date	Change Summary
1.0	09/02/2014	Rev 0.9 Preliminary to Rev 1.0 Production Release Updated start-up time specification Added typical operating plots Removed SOT23 package option Relabeled 25°C frequency spec as frequency tolerance Added Manufacturing Guidelines section
1.1	10/14/2014	Improved Start-up Time at Power-up spec Added 5pF LVCMOS rise/fall time spec
1.2	11/25/2014	Updated 5pF LVCMOS rise/fall time spec Added additional design-in/mfg guidelines
1.3	01/18/2018	Added 2nd landing pattern option Updated NanoDrive section Updated logo and company address, other page layout changes
1.4	03/20/2018	Corrected an error of the Pin Assignments in Figure 1